

High Performance Energy Efficient D Flip Flop Circuits

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Abstract—This paper work mainly deals with design and analysis of different Flip-Flops circuits for eliminating the redundant switching activity. These Flip-Flop circuits are simulated to evaluate their performance parameters in terms of total power dissipation, speed, and glitches at the output.

The logic style of the circuits used in the Flip-Flop's circuit architectures is based on CMOS process model. For any timing element circuits, reducing the speed and power dissipation are the important constraints. By changing the size of the transistors and reducing the transistor count of the circuit the delay, the dynamic and leakage power dissipation can be reduced.

Here we are comparing these proposed circuit designs by various author which produce the Flip-Flop outputs simultaneously with full output voltage swing. The NMOS and PMOS transistors are added to the basic circuits to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design and reducing the redundant switching activity.

Index Terms: Timing element, flip-flop, Switching activity, Low power, High speed, very large scale integration (VLSI).

1. INTRODUCTION

The D flip flop receives the destination from its ability to hold data into its internal storage. This type of flip flop is sometimes called a gated D latch. The CP input is often given the designation G to indicate that this input enables the gated latch to make possible data entry into the circuit.

The binary information present at the data input of the D flip flop is transferred to the q output when the CP input is enabled. The output follows the data input as long as the pulse remains in its 1 state.

When the pulse goes to 0, the binary information that was present at the data input at the time the pulse transition occurred is retained at the Q output until the pulse input is enabled again. The characteristic table for the D flip flop is as shown in fig. 1 it shows that the next state of the flip flop is independent of the present state since $Q(t+1)$ is equal to input D whether Q is equal to 0 or 1. This means that an input pulse will transfer the value of input D into the output of the flip-flop independent of the value of the output before the pulse was applied.

The characteristic equation shows clearly that $Q(t+1)$ is equal to D.

$$Q(t+1)=D$$

Table 1: Characteristic Table of DFF

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

1.1 MASTER SLAVE D FLIP FLOP:

A master slave flip is constructed from two flip flops. One circuit serves as a master and the other as a slave, and the overall circuit is referred to as a master slave flip flop. The logic diagram of a D master slave flip flop is shown in fig 1. It consists of-

A master flip flop,

A slave flip flop, and

An inverter.

When clock pulse CP is 0, the output of the inverter is 1. since the clock input of the slave is 1, the flip flop is enabled and the output Q is equal to Y, while Q' is equal to Y'. the master flip flop is disabled because because CP=0.

When the pulse becomes 1, the information then at the external D input is transmitted to the master flip flop. The slave flip flop is isolated as long as the pulse is at its 1 level, because the output of the inverter is 0.

When the pulse returns to 0, the master flip flop is isolated, which prevents the external inputs from affecting it. The slave flip flop then goes to the same state as the master flip flop.

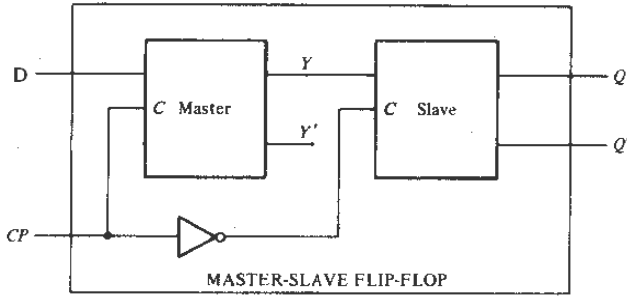


Fig. 1: Master Slave D Flip Flop Symbol

1.2 BASIC BUILDING BLOCKS OF MASTER SLAVE D FLIP FLOP

There are two major components of the master slave D flip flop. These are transmission gate and inverter.

a) Transmission gate

The transmission gate is on when $V_{en}=5V$ and $V_{enb}=0V$, assuming the bulk of MOS .Pis connected to $VDD(=5V)$ and the bulk of NMOS is connected to $GND(=0V)$ the on condition the output signal “out” will follows the input signal “in”. The operation of each transistor will first be analyzed. The NMOS switch will be analyzed by disconnecting the PMOS switch from the circuit. The source is connected to the input “in”, due to symmetrical structure of MOS transistor the source drain is not determined until the voltages are applied to the transistor. For NMOS the drain is connected to a higher potential than the source. In the circuit when the switch is on, the output $V(out)$ follows the input $V(in)$. That is, the $V(out)$ is approximately equal but slightly less than $V(in)$. Therefore, the source is connected to the “out” and $VDS=V(out)-V(in)\cong 0$. With a small VDS , the conducting NMOS transistor will be operating in the ohmic or non-saturated region. The NMOS will remain conducting as long as the gate source voltage exceed the threshold voltage, $V_{GS}\geq V_T$. Since the bulk is not connected to the source, the bulk effect will increase the threshold voltage to about 1.5V. The calculation of the threshold voltage will be shown later. As the input voltage $V(in)$ increases from 0 to 5V, the NMOS is on when $V_{GS} = V(en)-V(out)\cong V(en)-V(in)=5-V(in)\geq 1.5$ or $V(in)\leq 3.5V$. That is the NMOS switch will shut off when $V(in)\geq 3.5V$. can be verified using Pspice simulation. In the Pspice coding, S and D is interchangeable. The code is given in listing 1(a). The 1G load resistance is required by Pspice to prevent a floating output node.

$$V_{DS}=5$$

$$V_{GS} = V_G - V_S = 5 - 3.5 = 1.5$$

$$V_{BS} = V_B - V_S = 0 - 3.5 = -3.5$$

The following p

$$V_{TON}=V_{TO}=0.8630$$

(b) Inverter

The CMOS inverter is a basic building block for digital circuit design. the inverter performs the logic operation of A to A' . when the input to the inverter is connected to ground, the output, in accord with the digital models is pulled to 5v through the p channel transistor. When the input terminal is connected to vdd, the output is pulled to ground through the n channel MOSFET. The CMOS inverter has several important characteristics that are addressed. Its output voltage swing from vdd to ground unlike other logic families that never quite reach the supply levels, the static power dissipation of the CMOS inverter is zero. The inverter can be sized to give equal sourcing and sinking capabilities, and the logic switching threshold can be set by changing the size of the device

2. DESIGN TECHNIQUES

There are following five different types of design techniques of negative edge triggered D Flip Flop.

1. Conventional D Flip Flop.
2. Low-area D Flip Flop.
3. Low-power D Flip Flop.
4. Push-pull D Flip Flop.
5. Push-pull Isolation D Flip Flop.

All these design techniques have been developed for High performance energy efficient D Flip flop. The Energy is the product of average power consumed by the circuit and delay(C to Q).

2.1. CONVENTIONAL D FLIP FLOP

A conventional negative edge-triggered DFF consisting of two-level sensitive latches or 16 MOSFET’s is illustrated in Fig. 2 .

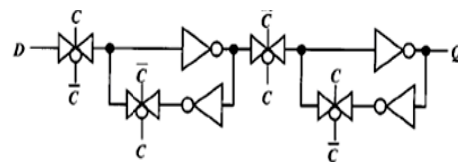


Fig. 2: Conventional D Flip Flop

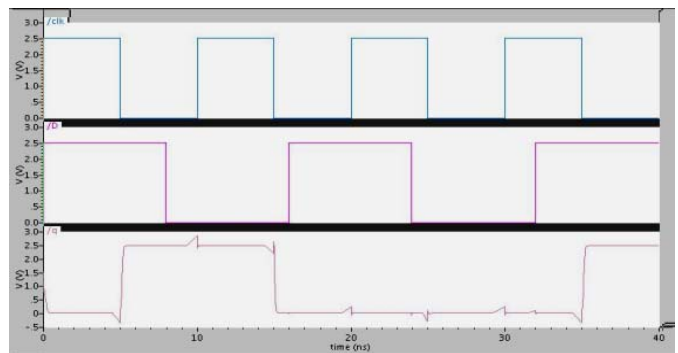


Fig. 3: Timing relationship in Conventional DFF

The speed of this conventional DFF is limited by two gate delays [one transmission gate and one inverter in Fig. 2, or 182.67 ps in Table 2] after the clock signal C transitions from logic 1 to 0. The advantage of this DFF design is that it involves minimum design risk.

2.2. LOW-AREA D FLIP FLOP

A common approach for reducing area overhead of the conventional DFF is to remove the two feedback transmission gates. This low-area DFF is depicted in Fig. 4. Although the strength of feedback inverters has been weakened to minimize short-circuit power dissipation due to voltage contention, this low-area DFF still consumes 18% more total power and is 42% slower (or has 76% more energy, Table 2) compared to the conventional DFF.

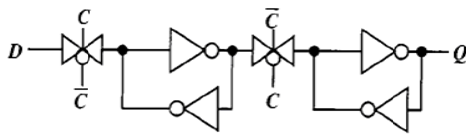


Fig. 4. Low-area D Flip Flop

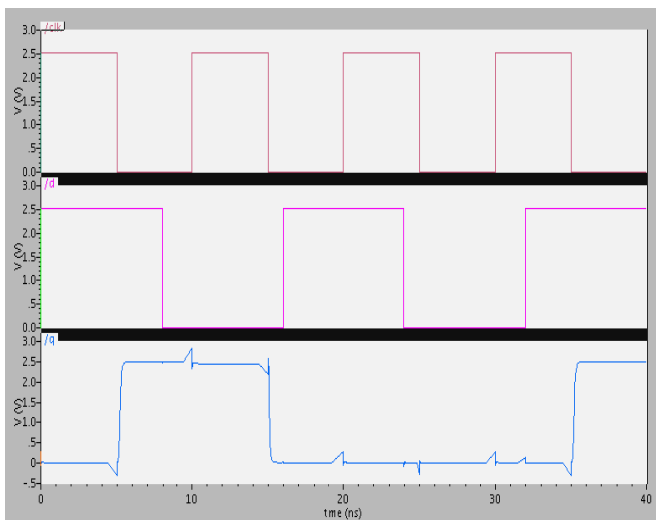


Fig. 5: Timing relationship of Low-area DFF

2.3. LOW-POWER D FLIP FLOP

One approach to optimize for power dissipation is to replace the inverter and transmission gate in the feedback path of Fig. 6 with a single tri-state inverter. This approach is referred to as a low-power DFF and was recently proposed by Gerosaet al. in [4]. Fig. 6 depicts this low-power DFF.

The tri-state inverter eliminates short-circuit power dissipation from the feedback path and yields only 1% reduction in total power and 3% (Table 2) slower speed when compared to the conventional DFF.

Considering area and energy efficiency, the low power DFF is comparable to the conventional DFF.

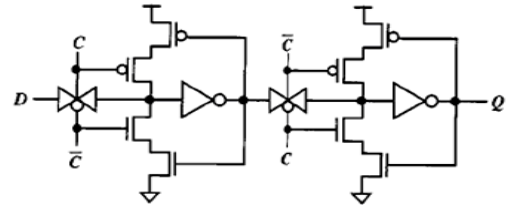


Fig. 6: Low-power D Flip Flop

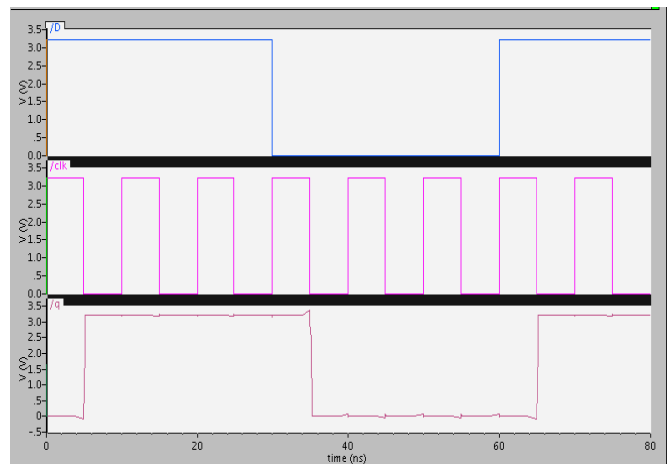


Fig. 7: Timing relationship of Low-power DFF

2.4. PUSH-PULL D FLIP FLOP

In order to improve performance of a conventional DFF, we propose addition of an inverter and transmission gate between the outputs of master and slave latches to accomplish a push-pull effect at the slave latch, i.e., input and output of the output inverter (which drives the signal Q directly) will be driven to opposite logic values during switching. This push-pull DFF is depicted in Fig. 9. This adds four MOSFET's, but reduces the clock-to-output (C-to-Q) delay from two gates in a conventional DFF to one gate.

One method to reduce the transistor count is to use an nMOSFET for latch input. However, since the output of an nMOSFET can only reach a voltage level of Vdd when it is at logic 1, it results in increased power dissipation. Therefore, a full transmission gate is kept in the push-pull DFF. To offset the four added MOSFET's for a push-pull DFF, we propose the elimination of two transmission gates from the feedback paths, as shown in Fig. 8.

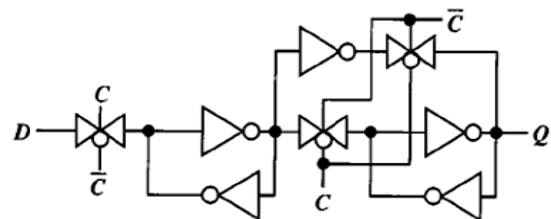


Fig. 8: Push-pull D Flip Flop

Compared to the conventional DFF, this push-pull DFF is 31% faster, but has a 22% power overhead.

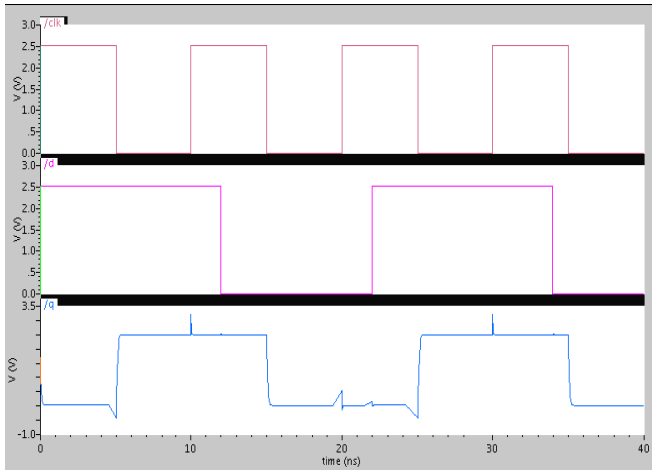


Fig. 9: Timing relationship of Push-pull DFF

2.5. PUSH-PULL ISOLATION D FLIP FLOP:

To optimize the proposed push-pull DFF for energy usage, we add two pMOSFET’s to isolate the feedback path, as illustrated in Fig. 10.

This PPI-DFF increases the transistor count to 18, but achieves a 16% reduction in total power dissipation and a speedup of 25% (Table 2) relative to the previous push-pull DFF in Fig. 8. Compared to the conventional DFF, PPI-DFF improves speed by 56% at an expense of 6% more power. Energy efficiency of this PPI-DFF is enhanced by 45–122% when compared to the previous four DFF’s. Further adding two N MOSFET’s to the feedback path of PPI-DFF (to make its feedback path identical to that of the conventional DFF) increases the transistor count to 20 and the load on clock signals. This derivative increases the total power dissipation by 9% and slows down C-to-Q delay by 12% relative to the PPI-DFF.

Applying a DPL input to the PPI-DFF can result in a 20% reduction in the setup time. However, when D is at logic 1 and C switches from logic 1 to 0, a dc path exists (INV2-P2-PI-C), leading to a 60% power overhead. Another option is to use a tri-state inverter to replace the push-pull driver of PPI-DFF,

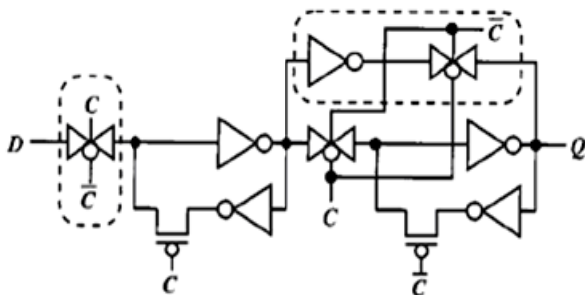


Fig. 10: Push-Pull Isolation D Flip Flop

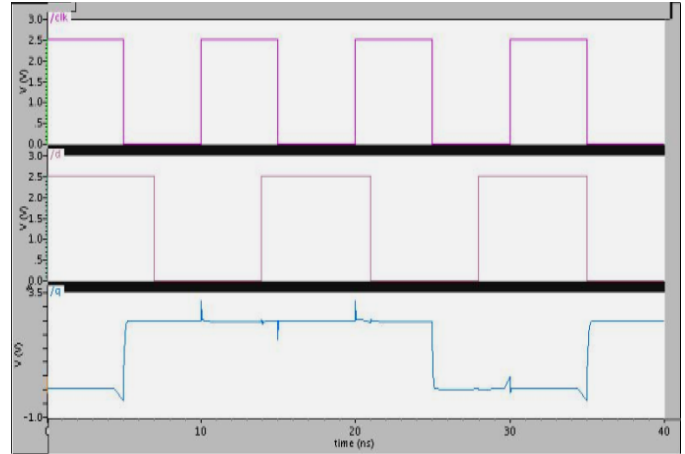


Fig. 11: Timing relationship of Push-pull Isolation DFF

Though this approach reduces the short-circuit power of the push-pull driver, it weakens the drive strength due to stacked MOSFET’s and is 10% less efficient in energy compared to the PPI-DFF.

Hence, compared to all the DFF’s and their derivations discussed above, the PPI-DFF turns out to be the most energy efficient.

3. COMPARISION PARAMETER

There are three parameters to compare the different types of D flip flop. These are :

1. Average Power: It is the average power consumed by the circuit.
2. Delay :It is the propagation delay from clock(C) to output(Q)
3. Energy :It is the product of average power and delay.

Table 2: Comparison of various D Flip Flops

Parameters	Conventional DFF	Lowarea DFF	Low-power DFF	Push-pull DFF	Push-pull Isolation
No. of Transistor	16	12	16	16	18
Avg. Power Percentage	130.69	168.00	125.04	171.23	144.94
Delay Percentage	90.16	115.91	86.27	118.23	100
Energy Percentage	182.67	252.12	218.64	157.64	134.23
Percentage	136.08	187.82	162.88	117.44	100
Energy Percentage	23.87	42.35	27.33	26.99	19.45
Percentage	122.72	217.73	140.51	138.76	100

4. CONCLUSION

It is clear from the Table 2. that among the five DFF proposed push-pull isolation DFF is fastest with best energy efficiency but with drawback that it uses maximum no of transistor 18. Our proposed PPI-DFF improves speed by 36% at the expense of only 10% more power, when compared to a conventional

DFF. Energy efficiency of this PPI-DFF is 22–117% better than that of the other DFF's. Compared to the existing low-power DFF [4], our PPI-DFF uses 40% less energy. This may result in a 30–40% reduction in the overall energy consumption of control logic.

Though the low-area DFF uses up to 33% fewer transistors, the internal voltage contention consumes up to 122% more energy than the rest of DFF's. Compared to a conventional DFF, a low-power and a push–pull DFF improve power dissipation by 1% and delay by 31%, respectively, but end up with a comparable energy efficiency.

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